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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/682,277	10/08/2003	Darrell Rinerson	UNTYP024	9336

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 02/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/682,277	RINERSON ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *27 and 28* is/are allowed.

6)☒ Claim(s) *1-26 and 29-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's arguments with respect to claims 1-43, filed 05 August 2002, have been considered but they are moot in view of new ground(s) of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 38 and 41-42** are rejected under 35 U.S.C. 102(e) as being anticipated by Monsma et al. U.S. Patent 6,331,944 (the '944 patent).

The '944 patent discloses in Figures 2's and respective portions of the specification a conductive memory device as claimed.

Referring to **claim 38**, the '944 patent discloses a conductive memory device, comprising:

a memory element (100) that stores an adjustable resistive value;

two electrodes (23/24/25/16 and 22) that deliver current to the memory element;

wherein at least one electrode includes a terminal layer (23 or 22) that is suitable for connecting the electrode to a conductive line (3);

wherein the at least one electrode has an outside face that is defined by the terminal layer (23) and an inside face opposite the outside face; and

wherein the at least one electrode ("MBM" element 23/24/25/16 – see note below) acts as a barrier layer (24); and

wherein at least one electrode (23/24/25/16) acts as a seed layer ("template layer" 16).

Using the same reference characters and citations as detailed above where applicable and with reference to **claim 41**, the '944 patent discloses a re-writable memory comprising:

a substrate (not shown but is inherent for the memory to function);

a plurality of circuits (not shown) on the substrate;

a plurality of x-direction conductive lines (1...3) oriented in one direction;

a plurality of y-direction conductive lines (4...9) in a different direction as the x-direction conductive lines, and crossing the x-direction conductive lines; and

at least one memory array having memory cells located substantially at the intersections of the x-direction conductive lines and y-direction conductive lines;

wherein each of the memory cells in the memory array includes at least one electrode that acts as a barrier layer; and

wherein each of the memory cells in the memory array includes at least one electrode that acts as a seed layer to at lest a portion of the memory cell.

It is noted that the '944 patent's MBM element 23/24/25/16 is not exactly termed an electrode, however, its structure and function – the thickness of the layer B (24) is thin enough for direct electron tunneling – meet the broad definition of "electrode" (column 5, lines 19-24).

Referring to **claim 42**, MRAM cells comprise an adjustable resistive value as determined by the relative magnetic-vector orientations of the magnetic layers.

3. **Claims 38 and 41-42** are rejected under 35 U.S.C. 102(e) as being anticipated by Slaughter et al. U.S. Patent 6,544,801 (the '801 patent).

The '801 patent discloses in the figures, particularly Figures 5-7, and respective portions of the specification a conductive memory device as claimed.

Referring to **claim 38**, the '801 patent discloses a conductive memory device, comprising:

a memory element (30, or 50, or 54) that stores an adjustable resistive value;

two electrodes (22 or 54 or 72/74/76/78 and 29 or 67/68 or (not-shown)) that deliver current to the memory element;

wherein at least one electrode includes a terminal layer (22 or 72) that is suitable for connecting the electrode to a conductive line (not shown, connecting lines ,bit lines, etc., column 3, lines 55-60);

wherein the at least one electrode has an outside face that is defined by the terminal layer and an inside face opposite the outside face; and

wherein the at least one electrode (72/74/76/78) acts as a barrier layer (diffusion barrier 74, column 5, last paragraph); and

wherein at least one electrode (72/74/76/78) acts as a seed layer (76/78, column 6, lines 22-30).

Using the same reference characters and citations as detailed above where applicable and with reference to **claim 41**, the '801 patent discloses a re-writable memory comprising:

a substrate (not shown but is inherent for the memory to function);

a plurality of circuits (not shown, see note below) on the substrate;

a plurality of x-direction conductive lines (not shown) oriented in one direction;

a plurality of y-direction conductive lines (not shown) in a different direction as the x-direction conductive lines, and crossing the x-direction conductive lines; and

at least one memory array having memory cells located substantially at the intersections of the x-direction conductive lines and y-direction conductive lines;

wherein each of the memory cells in the memory array includes at least one electrode that acts as a barrier layer; and

wherein each of the memory cells in the memory array includes at least one electrode that acts as a seed layer to at lest a portion of the memory cell.

Note that the not-shown components are disclosed in column 3, lines 46+: "large arrays, ..." and large arrays are known to include the not-shown components.

Referring to **claim 42**, MRAM cells comprise an adjustable resistive value as determined by the relative magnetic-vector orientations of the magnetic layers.

Claim Rejections - 35 USC § 102 and 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 8-10, 14, 17-26, 32, and 37 are rejected under 35 U.S.C. 102(e) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Ignatiev et al. U.S. Patent 6,473,332 (the '332 patent, cited in the previous Office Action).

The '332 patent discloses in Figure 1 and respective portions of the specification a conductive memory device as claimed or substantially as claimed. The '332 patent discloses an electrically operated, over-writable, multi-valued, non-volatile resistive memory element (Abstract), and a memory element array including a plurality of the memory elements formed on a substrate in a column-row or array format (column 2, lines 53-56), the memory element comprises a variable resistive element 110 sandwiched by a pair of electrodes 108 and 112, where the variable resistive element 110 is formed of CMR materials, perovskite materials, PCMO, LSMO, GBCO or other CMR oxide (column 7, lines 17-23, and column 8, lines 19-22), and the electrodes are formed of metals, metallic oxides, polymers, or mixtures or combinations thereof, Pt, Ag, Au, LaSrCoO.sub.3, YBa.sub.2 Cu.sub.3 O.sub.7-x, RuO.sub.2, IrO.sub.2, SrRuO.sub.3, Al, Ta, TaSiN, MoN doped polyacetylene, polypyrrole, polyaniline, or mixtures or combinations thereof (column 7, lines 10-16).

The reference further discloses in column 7, lines 24-30, that: "other substrates which are known for use as atomic templates for the atomically ordered growth of the resistive CMR layer or the bottom electrode layer, or mixtures or combinations thereof" (emphasis added), which

conveys or appears to convey the meanings that the bottom electrode could be a seed layer (atomic template).

Specifically, with reference to **claim 1**, the '332 patent discloses a conductive memory device comprising:

a conductive bottom electrode (108);

a multi-resistive state element (110) arranged on top of and in contact with the bottom electrode, the multi-resistive state element having a resistivity; and

a conductive top electrode (112) arranged on top of and in contact with the multi-resistive state element;

wherein the resistivity of the multi-resistive state element may be changed by applying a first voltage having a first polarity across the conductive electrodes and reversibly changed by applying a second voltage having a second polarity across the conductive electrodes (Abstract), the second polarity being opposite to the first polarity (column 8, lines 40-50: "Pulses with negative polarity (negative pulse applied to the top electrode on the PCMO layer) resulted in a gradual and stepwise increase in resistance of the device to a high resistance saturation value. Pulses of opposite polarity (positive polarity) resulted in a gradual and stepwise decrease in resistance to a low resistance saturation value"); and

wherein at least one of the conductive electrodes (formed of a refractory metal nitride or a refractory metal oxide such as TaSiN, MoN, IrO_2, and RuO_2, as detailed above) functions as a barrier layer; and

wherein at least one of the conductive electrodes functions or appears to function as a seed layer (as noted above).

Note also that although the '332 patent does not explicitly disclose that the conductive electrodes formed of a refractory metal nitride or a refractory metal oxide function as a barrier layer, they function as a barrier layer as is known in the art and as will be explained in details in the paragraphs that follow.

Regarding **claims 8-10**, the '332 patent further discloses that the at least one of the conductive electrodes that functions as a barrier layer includes the ternary nitride TaSiN (tantalum silicon nitride) as claimed. And although not explicitly disclosed, the disclosed ternary nitride TaSiN, just as the claimed ternary nitride TaSiN, reduces either metal diffusion, oxygen diffusion, hydrogen diffusion, or some combination thereof.

Referring to **claims 14 and 18-19**, the '332 patent further discloses that the at least one of the conductive electrodes that functions as a barrier layer includes ternary oxide $SrRuO_3$ and that ternary oxide $SrRuO_3$, being included in the conductive electrode, is a conductive oxide although not explicitly disclosed.

Referring to **claim 21,** the limitation "is oxidized during fabrication" of "the conductive oxide is a conductive metal that is oxidized during fabrication" is taken to be a product-by-process limitation and is considered non-limitation in a product claim (MPEP 2112.01 and MPEP 2113). In a product-by-process claim, it is the patentability of the claimed product and not of the recited process steps which must be established. Therefore, when the prior art discloses a product, the ternary conductive oxide $SrRuO_3$, which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. The Patent Office is not equipped to manufacture products by a myriad of processes put before it and then obtain prior art product and make

physical comparisons therewith. As for the limitation "remains conductive after oxidation", the conductive oxide of the conductive electrode shall remain conductive for the device to function.

Referring to **claim 22**, as cited above, the metal is Ir or Ru.

Referring to **claim 32**, which recites: "the top electrode, the multi-resistive state element, and the bottom electrode each have similar coefficients of thermal expansion", the top electrode, the multi-resistive state element, and the bottom electrode of the conductive element of the '332 patent each is a metal oxide having an atomic weight similar to those of the others and therefore each has a coefficient of thermal expansion similar to those of the others, whereby the conductive memory element does not experience significant stress from dissimilar coefficients of thermal expansions during normal operation.

Referring to **claim 17**, as mentioned above, the '332 patent discloses ternary conductive oxides such as $SrRuO_3$, metals, metal oxides and mixtures and combinations thereof for conductive electrodes (108 or 112), and since the '332 patent does not exclude the use of a separate barrier layer (in addition to the conductive electrode layer), it would appear that the ternary oxide of the conductive electrode 108 or 112 could function as a sacrificial barrier (i.e., as a separate barrier layer), and since the disclosed ternary oxide and the claimed ternary oxide is of the same or similar material, the ternary oxide disclosed by the '332 patent would function as a high-temperature oxygen barrier. As for the limitation "at least one of the conductive electrodes remains conductive", the conductive electrodes should remain conductive for the device to function.

Referring to **claims 2 and 25**, since the materials or combinations of the materials of the '332 patent's device are similar to those used by the present invention, as cited above, the multi-resistive state element appears to be fabricated with high temperature processes.

Referring to **claim 20**, the '332 patent discloses RuO_2 , IrO_2, metal, metal oxides and mixtures and combinations thereof, as cited above, and since the reference does not exclude the possibility of the metal and the metal oxide being the same metal, it appears that the metal and the metal oxide could be the same metal.

With respect to the claimed limitations of claims **23-24 and 26**, the conductive oxide of the '332 patent, being formed of the same or similar materials as claimed, could function as claimed.

Referring to **claim 37**, although the '332 patent does not disclose that the at least one of the conductive electrodes that functions as a barrier layer is the bottom electrode and the top electrode is a non-oxidized metal, the reference teaches that, as cited above, suitable electrode materials include, without limitation, metals, metallic oxides, polymers, or mixtures or combinations thereof. Therefore, the at least one of the conductive electrodes (the metal oxide) that functions as a barrier layer could be the bottom electrode, and the top electrode could be a metal (a non-oxidized metal).

Referring to the limitation "a plurality of x-direction conductive lines in oriented in one direction; a plurality of y-direction conductive lines in a different direction as the x-direction conductive lines, and crossing the x-direction conductive lines; at least one memory array formed by memory cells placed substantially at the intersections of the x-direction conductive lines and y-direction conductive lines" of **claim 41**, as noted above, the '332 patent discloses a memory

element array including a plurality of the memory elements formed on a substrate in a column-row or array format. Thus, the memory array shall include X-conducting lines and Y-conducting lines and the cells should be placed substantially at the intersections of the x-direction conductive lines and y-direction conductive lines.

Referring to **claim 43**, each memory cell includes a conductive metal oxide memory element (such as PCMO as cited above) that stores an adjustable resistive value.

Claim Rejections - 35 USC § 103

5. **Claim 3-7, 11-13, 15-16, 29-30, 33-36, and 38-43** are rejected under 35 U.S.C. 103(a) as being unpatentable over the '332 patent for being obvious.

The '332 patent discloses a conductive memory device as claimed or substantially as claimed and as detailed above for claim 1 including a pair of electrodes sandwiching a multi-state resistive element, wherein the lower electrode is or appears to be a seed layer. The reference further discloses that the device could be formed in column-row or array format (column 2, lines 53-56) but neglects to disclose details such as a conductive line or x-direction conductive lines and y-direction conductive lines as recited in **claims 38 and 41**. Nevertheless, x-direction conductive lines and y-direction conductive lines as claimed are required to form the device in column-row or array format. For example, see Fig. 1A of the '944 patent, cited above, or Figs. 1 and 2 of Peterson U.S. Patent 5,930,162. It is therefore obvious to add these x-direction conductive lines and y-direction conductive lines and couple them to the electrodes as claimed.

Referring to **claims 3 and 4**, the '332 patent discloses a conductive memory device as claimed and as detailed above including the conductive electrodes (108 and 112), at least one of which functions as a barrier layer, but instead of using titanium nitride (TiN) as a material to form the at least one of the conductive electrodes as claimed, the '332 patent discloses using TaSiN. However, TaN or TaSiN functions as a diffusion barrier layer and an adhesive layer (see, for example, U.S. Patent 6,346,475 to Suzuki et al., cited in the previous Office Action, column 8, lines 15-18) and TiN and TaN (tantalum nitride) are known to function as an adhesive and a barrier layer (see, for example, U.S. Patent 5,668,054 to Sun et al., cited in the previous Office Action, in the Technical Background Section). Since TaN and TaSiN are art-equivalent materials and TiN and TaN are art equivalent materials, it follows that TaSiN and TiN are art-equivalent materials. Since the materials are art-equivalent, the change of the materials would have been obvious to one of ordinary skill in the art. Note also that all of these metal nitrides are refractory metal nitrides.

With respect to **claims 5-7**, similarly as detailed above being art-equivalent materials, the disclosed binary nitride MoN is functionally equivalent to the claimed titanium nitride or tantalum nitride as claimed (they are all refractory metal nitrides).

Referring to **claims 11-13**, the '332 patent discloses a conductive memory device as claimed and as detailed above including the ternary nitride conductive electrode (108 or 112) formed of TaSiN but the '332 patent's ternary nitride does not include one component that is either ruthenium or iridium and another component that is either tantalum or titanium, or to be specific, the '332 patent discloses TaSiN instead of RuTiN (ruthenium titanium nitride) as claimed. Nevertheless, either of the two ternary nitrides (TaSiN and RuTiN) functions as a

conductive barrier layer as is known in the art and as is disclosed by Choi U.S. Patent Application Publication 20030042609 (paragraph [0039]), as an example. Since the materials are art-equivalent, the change of the materials would have been obvious to one of ordinary skill in the art. As for the limitation "the ternary nitride functions as a sacrificial high-temperature oxygen barrier" of **claim 13**, since the '332 patent does not exclude the use of a separate barrier layer (in addition to the conductive electrode layer), it would appear that the ternary nitride of the conductive electrode 108 or 112 could function as a sacrificial barrier (i.e., as a separate barrier layer), and since the disclosed ternary nitride and the claimed ternary nitride is of the same or similar material, the ternary nitride disclosed by the '332 patent would function as a high-temperature oxygen barrier.

Referring to **claims 15-16**, the '332 patent discloses a conductive memory device as claimed and as detailed above including the ternary oxide conductive electrode (108 or 112) formed of $SrRuO_3$ but the '332 patent's ternary oxide does not have one component that is either ruthenium or iridium and another component that is either tantalum or titanium. To be specific, the '332 patent discloses $SrRuO_3$ instead of RuTa O_x (ruthenium tantalum oxide) as claimed. However, as should be apparent by now, $SrRuO_3$ and RuTa O_x, being refractory metal ternary oxides, are functionally equivalents.

Referring to **claims 29-30, 33-36, and 39-40**, the materials and the relative positions of the sub-layers of the electrodes are all within the skill of one in the art at the time the invention was made to select and arrange.

Referring to **claim 42**, as noted above for claim 1, the memory cell comprises an adjustable resistive value.

Referring to **claim 43**, the programmable complex conductive metal oxide of the '332 patent is a crystalline conductive material, and although not explicitly disclosed, the "atomic template" layer (seed layer as claimed) contributes to the crystalline structure of the conductive metal oxide.

6. **Claims 1, 3-12, 14-16, 18-24, 26, 29-37, and 39-40** are rejected under 35 U.S.C. §103(a) as being unpatentable over the '944 patent in view of knowledge in the pertinent art.

The '944 patent discloses a conductive memory device as claimed and as detailed above but fails to teach the particular mode of programming as claimed. Specifically, in reference to **claim 1**, the reference discloses a conductive memory device comprising:

a conductive bottom electrode (23/24/25/16);

a multi-resistive state element (17...21, "MTJ" or magnetic tunnel junction) arranged on top of and in contact with the bottom electrode, the multi-resistive state element having a resistivity; and

a conductive top electrode (22) arranged on top of and in contact with the multi-resistive state element;

wherein the resistivity of the multi-resistive state element may be changed by applying a first voltage having a first polarity across the conductive electrodes and reversibly changed by applying a second voltage having a second polarity across the conductive electrodes; and

wherein at least one of the conductive electrodes functions as a barrier layer (24); and

wherein at least one of the conductive electrodes (23/24/25/16) functions as a seed layer ("template layer" 16).

However, the reference fails to disclose that the second polarity is opposite to the first polarity. Nevertheless, in the magnetic random access memory (MRAM) art, at the time the invention was made, there were two modes to program (to change the resistive state of the MRAM) the cells (elements). As disclosed by Savtchenko et al. U.S. Patent 6,545,906, in the paragraph bridging columns 3 and 4, MRAM cells resistive state could be changed by applying a voltage of opposite or the same polarity. Therefore, it appears that the limitation "the second polarity is opposite to the first polarity" is one of various methods one of ordinary skill in the art would use to change resistive states and therefore would have been obvious.

Referring to **claims 18, 29, and 31**, the reference further discloses that (claim 18) the conductive electrode (23/24/25/16) that functions as a barrier layer includes a conductive oxide (TiO_2 24, column 6, lines 9-12), that (claim 29) the at least one of the conductive electrodes that functions as a barrier layer includes a layer of metal (25) in between the conductive oxide and the multi-resistive state element, and that (claim 31) the layer of metal introduces a non-linearity in the IV characteristics of the conductive memory device (column 5, lines 23-25: "non-linear current-voltage characteristic").

Referring to **claim 37**, the reference discloses that the at least one of the conductive electrodes that functions as a barrier layer is the bottom electrode and the top electrode is a non-oxidized metal (Pt, 22).

Referring to **claims 3-12, 14-16, 19-24, 26, 30, 32-36, and 39-40**, as detailed above in paragraphs numbered 4 and 5, the materials, names, intended functions, and relative positions of the sub-layers of the bottom electrode are within the ordinary skill of one in the art at the time the invention was made to select and therefore would have been obvious.

7. **Claims 1-26, 29-30, 32-37, and 39-40** are rejected under 35 U.S.C. §103(a) as being unpatentable over the '801 patent in view of knowledge in the pertinent art.

The '801 patent discloses a conductive memory device as claimed and as detailed above for claims 38 and 41 but fails to teach the particular mode of programming as claimed. Specifically, in reference to **claim 1**, the reference discloses a conductive memory device comprising:

a conductive bottom electrode (72/74/76/78, Fig. 7);

a multi-resistive state element (24...28, Fig. 5, "MTJ" or magnetic tunnel junction) arranged on top of and in contact with the bottom electrode, the multi-resistive state element having a resistivity; and

a conductive top electrode arranged on top of and in contact with the multi-resistive state element;

wherein the resistivity of the multi-resistive state element may be changed by applying a first voltage having a first polarity across the conductive electrodes and reversibly changed by applying a second voltage having a second polarity across the conductive electrodes; and

wherein at least one of the conductive electrodes functions as a barrier layer (74); and

wherein at least one of the conductive electrodes functions as a seed layer (76/78).

However, the reference fails to disclose that the second polarity is opposite to the first polarity. Nevertheless, in the magnetic random access memory (MRAM) art, at the time the invention was made, there were two modes to program (to change the resistive state of the MRAM) the cells (elements). As disclosed by Savtchenko et al. U.S. Patent 6,545,906, in the

paragraph bridging columns 3 and 4, MRAM cells resistive state could be changed by applying a voltage of opposite or the same polarity. Therefore, it appears that the limitation "the second polarity is opposite to the first polarity" is one of various methods one of ordinary skill in the art would use to change resistive states and therefore would have been obvious.

Referring to **claims 2 and 25**, the reference further discloses that the multi-resistive state element is fabricated with high temperature processes (column 4, lines 15-25 and column 6, lines 30-34).

Referring to **claims 3-24, 26, 29-30, 32-36, and 39-40**, the reference further discloses that the at least one of the conductive bottom electrodes that functions as a diffusion barrier layer include a material such as tantalum oxide, tantalum nitride, or aluminum oxide, aluminum nitride, etc. (column 5, last paragraph). As for the conductive materials that the reference neglects to disclose, as detailed above in paragraphs numbered 4 and 5, the materials, names, intended functions, and relative positions of the sub-layers of the bottom electrode are within the ordinary skill of one in the art at the time the invention was made to select and therefore would have been obvious.

Allowable Subject Matter

8. **Claim 27 and 28** are allowable over the prior art of record. The allowable subject matter was indicated in the previous Office Action, and note the limitations "all", "barrier layer", seed layer, and "conductive oxide" in the indication.

Conclusion

9. Applicant's amendment, which results in new limitations and new combinations of limitations, necessitated the new ground(s) of rejection presented in this Office Action. See MPEP § 706.07(a).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
January 25, 2005

David Nelms
Supervisory Patent Examiner
Technology Center 2800